

PATENT

Atty. Dkt. No. YOR920030469US1

**IN THE CLAIMS**

1. (Currently Amended) A method of fabricating a complementary metal oxide semiconductor (CMOS) field effect transistor, comprising the steps of:
  - (a) providing a substrate;
  - (b) providing on said substrate a polysilicon layer formed upon a gate dielectric layer ~~of a gate structure of the transistor~~;
  - (c) doping the polysilicon layer using at least one dopant;
  - (d) ~~forming a polysilicon gate electrode of the gate structure~~ forming a gate structure for the transistor having a polysilicon gate electrode and raised source and drain regions;
  - (e) depositing on the polysilicon gate electrode at least one of a metal and an alloy; and
  - (f) siliciding the polysilicon gate electrode to form a silicide and at least one monolayer of the at least one dopant at an interface between the gate dielectric layer and the silicide.
2. (Original) The method of claim 1, wherein the doping step (c) is performed after the forming step (d).
3. (Original) The method of claim 1, wherein the at least one dopant comprises at least one of As, P, B, Sb, Bi, In, Tl, Al, Ga, Ge, Sn and N<sub>2</sub>.
4. (Original) The method of claim 1, wherein the doping step (c) dopes the polysilicon layer using Sb as said at least one dopant.
5. (Original) The method of claim 1, wherein the doping step (c) dopes the polysilicon layer using an ion implantation process.
6. (Original) The method of claim 5, wherein the doping step (c) dopes the polysilicon layer using a pre-determined dose in a range from about  $1 \times 10^{14}$  to  $4 \times 10^{15}$  ions/cm<sup>2</sup>.

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7. (Original) The method of claim 1, wherein the forming step (d) further comprises the step of:

amorphizing the polysilicon gate electrode.

8. (Original) The method of claim 7, wherein said amorphizing step comprises the step of:

performing an ion implantation process using at least one of Si and Ge.

9. (Original) The method of claim 1, wherein said at least one of the metal comprises at least one of Ni, Co, Pt, Ti, Pd, W, Mo, and Ta.

10. (Original) The method of claim 1, wherein said at least one of the metal comprises Ni.

11. (Original) The method of claim 1, wherein said at least one of the metal comprises Co.

12. (Original) The method of claim 1, wherein said at least one of the alloy comprises at least one of C, Al, Ti, V, Cr, Mn, Fe, Co, Ni, Cu, Ge, Zr, Nb, Mo, Ru, Rh, Pd, Ag, In, Sn, Hf, Ta, W, Re, Ir, and Pt.

13. (Original) The method of claim 1, wherein said siliciding step employs an annealing process.

14. (Original) The method of claim 13, wherein the annealing process is performed at a substrate temperature of about 350 to 750 degrees Celsius for a duration of about 0.3 to 30 min.

15-30. (Cancelled)